CLAIMS

What is claimed is:

1. A processor comprising:

a set of general purpose registers; and

a set of exception registers that are switched for at least a subset of said set of general purpose registers when an exception occurs.

2. The processor of Claim 1, wherein said set of exception registers is a dedicated set of registers for servicing exceptions.

3. The processor of Claim 2, wherein said set of exception registers is for servicing exceptions having a high priority.

4. The processor of Claim 2, wherein said processor provides a dedicated vector to said set of exception registers for said exception.

5. The processor of Claim 1, wherein there are at least eight exception registers.

6. The processor of Claim 1, wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls.

7. The processor of Claim 6, wherein said processor provides a first dedicated vector to software which uses said portion of said set of exception registers for interrupts and a second dedicated vector to software which uses said another portion of said set of exception registers for servicing operating system calls.

8. The processor of Claim 1, further comprising:

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a select logic circuit having a first input terminal that receives an exception register active bit and a second input terminal that receives a register address bit, said select logic circuit provides an output signal on an output terminal used to select between said set of general purpose registers and said exception registers.

9. A method of interrupting the execution of a task and servicing an exception in a processor, said method comprising:

asserting an exception;

swapping a set of general purpose registers for at least one set of exception registers;

servicing said exception using said at least one set of exception registers; and

swapping out said exception registers for said set of general purpose registers and resuming execution of said task.

10. The method of Claim 9, wherein said at least one set of exception registers is a dedicated set of exception registers.

11. The method of Claim 9, wherein servicing said exception using said at least one set of exception registers comprises modifying the values of the registers in said set of exception registers without disrupting the state of the interrupted task.

12. The method of Claim 9, wherein said exception is a high priority exception, said method further comprising:

providing a first vector and activating said at least one set of exception registers for said high priority exception; and

providing a second vector and not activating said set of exception registers for lower priority exceptions.

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13. The method of Claim 12, wherein said first vector is a dedicated vector and said providing said first vector automatically separates said high priority exception from said lower priority exceptions.

14. The method of Claim 9, wherein said exception is a high priority exception and is either an interrupt or an operating system call, said method further comprising:

providing a first vector and activating at least a portion of said exception registers for said high priority exception when said exception is an interrupt;

providing a second vector and activating at least another portion of said exception registers for said high priority exception when said exception is an operating system call; and

providing a third vector and not activating said set of exception registers for lower priority exceptions.

15. The method of Claim 14, wherein said first vector and said second vector are dedicated vectors and said providing said first vector and providing said second vector automatically separates said high priority exception from said lower priority exceptions.

16. An apparatus for executing tasks and servicing exceptions, said apparatus comprising:

means for interrupting a task when an exception is asserted;

means for servicing said exception without disrupting the state of the interrupted task; and

means for resuming execution of said interrupted task.

17. The apparatus of Claim 16, wherein:

said means for servicing comprises a means for activating at least one set of exception registers; and

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means for resuming execution of said interrupted task comprises a means for deactivating said exception registers and activating general purpose registers to resume execution of said task.

18. The apparatus of Claim 17, wherein said means for activating comprises a first select logic circuit coupled to said set of general purpose registers and a second select logic circuit coupled to said at least one set of exception registers, said second select logic circuit receives an execution register active bit enabling said at least one set of exception registers and said second select logic circuit receives an inverted execution register active bit disabling said set of general purpose registers.

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